AMENDMENT TO THE CLAIMS

*Please cancel claims 1-24 without prejudice or disclaimer of the subject matter recited therein.* Applicants expressly reserve the right to file one or more continuation applications directed to the subject matter recited therein; *and*

*Please add new claims 32-48:*

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Claims 1-30 (Canceled).

Claim 31. (Previously Presented) A method of fabricating a semiconductor structure, comprising the steps of:

forming a $Si_{1-x}Ge_x$ layer on a multi-layer substrate;

forming a plurality of channels in the $Si_{1-x}Ge_x$ layer and in a top layer of the multi-layer substrate;

after forming the plurality of channels, removing the top layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the multi-layer substrate; and

filling the channels and the void with a dielectric material.

Claim 32. (New) The method of claim 31, wherein the dielectric material comprises silicon dioxide.

Claim 33. (New) The method of claim 31, further comprising, after the forming of the $Si_{1-x}Ge_x$ layer, forming a cap layer on the $Si_{1-x}Ge_x$ layer.

Claim 34. (New) The method of claim 33, wherein the forming of a plurality of channels comprises forming a plurality of channels in the cap layer, the $Si_{1-x}Ge_x$ layer, and the top layer of the multi-layer substrate.

Claim 35. (New) The method of claim 31, further comprising removing the cap layer after the filling of the channels and the void with the dielectric material.

Claim 36. (New) The method of claim 31, further comprising removing a cap layer arranged above the $Si_{1-x}Ge_x$ layer after the filling of the channels and the void with the dielectric material.

Claim 37. (New) The method of claim 36, further comprising forming a strained Si layer on the $Si_{1-x}Ge_x$ layer.

Claim 38. (New) The method of claim 36, wherein the forming of the strained Si layer is a step that includes one of:

ultrahigh vacuum chemical vapor deposition (UHVCVD);

rapid thermal chemical vapor deposition (RTCVD);

low-pressure chemical vapor deposition (LPCVD)

limited reaction processing CVD (LRPCVD); or

molecular beam epitaxy (MBE).

Claim 39. (New) The method of claim 36, wherein the strained Si layer is comprised of a semiconductor comprising one of Si or $Si_{1-y}C_y$.

Claim 40. (New) The method of claim 36, further comprising forming additional $Si_{1-x}Ge_x$ on the $Si_{1-x}Ge_x$ layer to form a thicker $Si_{1-x}Ge_x$ layer.

Claim 41. (New) The method of claim 40, further comprising forming a strained Si layer on the thicker $Si_{1-x}Ge_x$ layer.

Claim 42. (New) The method of claim 31, wherein the semiconductor structure is one of a nFET and a pFET.

Claim 43. (New) The method of claim 31, wherein the plurality of channels include at least a first channel and a second channel and wherein the void is formed underneath the $Si_{1-x}Ge_x$ layer extending from at least the first channel to the second channel.

Claim 44. (New) The method of claim 31, wherein the removing the top layer of the multi-layer substrate underneath the $Si_{1-x}Ge_x$ layer to form a void defined by an undercut border in the multi-layer substrate includes one of:

etching underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching underneath the $Si_{1-x}Ge_x$ layer;

performing timed etching underneath the $Si_{1-x}Ge_x$ layer using an etchant that exhibits a higher etch rate for the multi-layer substrate than for $Si_{1-x}Ge_x$; and

performing timed etching underneath the $Si_{1-x}Ge_x$ layer using an etchant from a group consisting of ammonia, tetramethyl ammonium hydroxide, nitric acid and hydrofluoric acid.

Claim 45. (New) The method of claim 31, wherein the $Si_{1-x}Ge_x$ layer has a bottom surface and a top surface, and the bottom surface is more resistant to etching than the top surface.

Claim 46. (New) The method of claim 45, wherein the $Si_{1-x}Ge_x$ layer has a higher concentration of Ge at the bottom surface than at the top surface.

Claim 47. (New) The method of claim 31, further comprising thermal annealing the $Si_{1-x}Ge_x$ layer after the filling of the channels and the void with the dielectric material.

Claim 48. (New) The method of claim 31, further comprising planarization after the filling of the channels and the void with the dielectric material.